High-performance CMOS current comparator

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A new high-performance CMOS current comparator is proposed. By adding two inverters in the feedback loop of Traff's comparator, the proposed comparator exhibits significant speed improvement especially for low input currents. Simulated in a 0.18 µm CMOS technology, the comparator achieves a 0.6 ns delay for a 100 nA input current at 1.8 V supply, which is about eight times faster than Traff's comparator.

Introduction: The current-mode technique, which is compatible with low supply voltage and standard digital CMOS processes, has been found useful in many applications [1]. As a critical component for current-mode circuits, the current comparator has received considerable attention. The desired features of a current comparator include high speed, low input impedance, low power and low supply voltage. Among these requirements, the speed for low current levels is very critical in many situations since it can be the limiting factor of the overall speed of a system. For instance, the speed of a current-mode A/D converter is limited by the response time of the comparator at its minimum input current levels for a given possibility of metastability error.

![Schematic diagrams of Traff's circuit and proposed circuit](image)

Fig. 1 Schematic diagrams of Traff’s circuit and proposed circuit

a Traff’s circuit  
b Proposed circuit

The first low input impedance current comparator was reported by Traff [2], which is perhaps the closest to a true current comparator compared to conventional comparators based on current mirrors. However, as pointed out in [3], Traff’s comparator encounters long response time for low input currents, which limits its performance. Remedies to this problem were reported in [3] and [4]. The one in [3] adds constant current biasing circuits to bias input transistors in class AB operation and the one in [4] uses a pair of diode-connected NMOS and PMOS transistors to prevent the input transistors from entering deep subthreshold state. The former method substantially increases circuit complexity and requires a twin-tub CMOS technology. The latter needs to stack two diode-connected transistors with very wide widths and is thus not suitable for low supply voltages. Last, the latest current comparator, reported in [5], achieves low-power performance, but its input node has a rail-to-rail voltage swing and is not a low impedance node indeed.

In this Letter, we present a new design with a fast response time and low input impedance by adding two inverters to Traff’s topology. The new technique is also suitable for low supply voltages.

Proposed current comparator: Fig. 1a shows the Traff comparator circuit. At the beginning of the comparison, input transistors Mn1 and Mp1 are in deep subthreshold (OFF) state. When a low input current comes in, the input of inverter A1 is charged or discharged slowly and V(1) changes slowly too. So it needs a long time to turn on Mn1 or Mp1 and then to activate the feedback. To overcome this disadvantage, in the proposed circuit shown in Fig. 1b we introduce inverters A2 and A3, together acting as a non-inverting amplifier, in the feedback loop. For a low input current, there are small voltage changes at the input node and node 1 for a short time, as that in Traff’s. But owing to the amplification by A2 and A3, V(2) changes substantially, turning on Mn1 or Mp1 and activating the feedback loop. Hence the response time is sharply reduced. To frequency-compensate the multi-stage amplifier formed by A1, A2 and A3, a small capacitor and resistor are used. Furthermore, the input impedance of the new circuit, given by

\[ R_{innew} = \frac{1}{g_{mT}(1 + G_1 G_2 G_3)} \]

is much lower than that in Fig. 1a, which has the value:

\[ R_{intraff} = \frac{1}{g_{mT}(1 + G_1)} \]

where \( g_{mT} \) is the transconductance of Mn1 or Mp1 and G1, G2 and G3 are the voltage gain of the inverter amplifier A1, A2 and A3, respectively.

Seen from above, the required voltage fluctuation at V(1) to turn on or off the input transistor is reduced in the proposed comparator. To get a rail-to-rail output voltage, three more inverters are added after V(1), the same as the case in the comparators in [3] and [4]. However, the delay introduced by the additional inverters can be neglected for low input currents since the response time of the earlier part of the comparator is much longer than the propagation delay of the inverters.

The added inverters will slightly increase power consumption, compared to Traff’s circuit. But the speed is improved significantly for low input currents, which is more important in many applications. Compared to the comparators in [3] and [4], the proposed circuit is much simpler and more suitable for low voltage operation.

Simulation results: To verify the proposed technique, the new comparator and Traff’s one were simulated in a 0.18 µm CMOS technology. In the simulation setting, all n-channel MOSFETs are 0.24/0.18 µm, and all p-channel MOSFETs are 1.2/0.18 µm. The compensation capacitor C and resistor R are 0.1pF and 10 KΩ respectively. The results reported below are for a 1.8 V supply. Similar performance improvement was also achieved for a 1.2 V supply with a differently sized comparator.

Fig. 2 shows the simulated signal waveforms when a square-wave input current with 100 nA amplitude is applied. As can be seen, the input node of the new comparator has a reduced voltage swing, which is in line with the analysis. When the input current changes from -100 to 100 nA, the proposed comparator has a response time (defined as the time interval between the zero input current point and the point when v(output) reaches Vdd/2) of 0.6 ns, only about an eighth of that of Traff’s.

![Transient waveforms for proposed and Traff’s comparators](image)

Fig. 2 Transient waveforms for proposed and Traff’s comparators

Fig. 3 shows the response time against input current amplitude for both comparators. It is observed that for low input currents (<10 µA),
the new comparator has more than a twofold speed improvement compared to Traff’s circuit. At large input currents ($I_{in} > 50 \mu A$), the speed improvement vanishes and the two comparators perform closely. This is mainly due to the fact that for large input currents the time taken for turning on the input transistor is very short for both comparators and in the proposed circuit the delay of the added inverters becomes a major part of the whole response time.

Conclusions: A new high-performance current comparator based on Traff’s circuit is presented. It achieves a much faster speed at low input current levels. With little circuit overhead introduced, the comparator also achieves low input impedance and is suitable for low voltage operation. Verified by transistor-level simulations, the proposed comparator can be used as an essential building block for a variety of current-mode systems, such as data converters and other front-end signal processing applications.

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